

IN THE CLAIMS

1. – 16. (Canceled)

17. (Currently Amended) A method of manufacturing a semiconductor device comprising:

forming a first insulating film on a semiconductor substrate;

forming wiring on the first insulating film wherein the wiring includes conductive film patterns and second insulating film patterns formed on the conductive film patterns;

forming a third insulating film on the wiring and the first insulating film using a silicon oxide based material;

planarizing the third insulating film until a surface of the second insulating film pattern is exposed;

forming contact patterns on the wiring wherein the contact patterns define contact hole regions;

forming contact spacers on sidewalls of the contact patterns; and

etching the third insulating film and the first insulating film using the contact patterns and the contact spacers as masks to form the contact holes and to simultaneously form third insulating film patterns on sidewalls of the wiring.

The method of claim 17, further comprising planarizing the third insulating film until a surface of the second insulating film pattern is exposed before forming the contact patterns.

18. – 24. (Canceled)

25. (Currently Amended) A method of manufacturing a semiconductor device comprising:

forming a first insulating film on a semiconductor substrate having capacitor contact regions;

forming bit lines on the first insulating film between the capacitor contact regions wherein the bit lines include first conductive film patterns and second insulating film patterns formed on the first conductive film pattern;

forming a third insulating film on the bit lines and on the first insulating film wherein the third insulating film includes a silicon oxide based material;

planarizing the third insulating film until surfaces of the second insulating film patterns are exposed;

forming contact patterns on the bit lines wherein the contact patterns define storage node contact hole regions;

forming contact spacers on sidewalls of the contact patterns; and

etching the third insulating film and the first insulating film using the contact patterns and the contact spacers as masks to form the storage node contact holes and to simultaneously form third insulating film patterns on sidewalls of the bit lines.

26. – 33. (Canceled)

34. (Currently Amended) A method of manufacturing a semiconductor device comprising:

forming a first insulating film on a semiconductor substrate having capacitor contact regions;

forming bit lines on the first insulating film between the capacitor contact regions wherein the bit lines include first conductive film patterns and second insulating film patterns formed on the first conductive film pattern;

forming a third insulating film on the bit lines and on the first insulating film wherein the third insulating film includes a silicon oxide based material;

forming contact patterns on the bit lines wherein the contact patterns define storage node contact hole regions;

forming a second conductive film on the contact patterns, the contact spacers and the storage node contact holes wherein the second conductive film fills up the storage node contact holes;

planarizing the second conductive film by a chemical mechanical polishing (CMP) process or an etch-back process when surfaces of the contact pattern are exposed to form storage node contact plugs in the storage node contact holes wherein the storage node contact plugs are connected to the capacitor contact regions;

forming contact spacers on sidewalls of the contact patterns; and

etching the third insulating film and the first insulating film using the contact patterns and the contact spacers as masks to form the storage node contact holes and to simultaneously form third insulating film patterns on sidewalls of the bit lines.

The method of claim 33, wherein the second conductive film is planarized when surfaces of the contact patterns are exposed.

35. (Currently Amended) A method of manufacturing a semiconductor device comprising:

forming a first insulating film on a semiconductor substrate having capacitor contact regions;

forming bit lines on the first insulating film between the capacitor contact regions wherein the bit lines include first conductive film patterns and second insulating film patterns formed on the first conductive film pattern;

forming a third insulating film on the bit lines and on the first insulating film wherein the third insulating film includes a silicon oxide based material;

forming contact patterns on the bit lines wherein the contact patterns define storage node contact hole regions;

forming a second conductive film on the contact patterns, the contact spacers and the storage node contact holes wherein the second conductive film fills up the storage node contact holes;

planarizing the second conductive film by a chemical mechanical polishing (CMP) process or an etch-back process until surfaces of the third insulating film patterns formed on the bit line are exposed to form storage node contact plugs in the storage node contact holes wherein the storage node contact plugs are connected to the capacitor contact regions;

planarizing a predetermined portion of the third insulating film positioned on the bit lines;

forming contact spacers on sidewalls of the contact patterns; and

etching the third insulating film and the first insulating film using the contact patterns and the contact spacers as masks to form the storage node contact holes and to simultaneously form third insulating film patterns on sidewalls of the bit lines.

~~The method of claim 33, further comprising planarizing a predetermined portion of the third insulating film positioned on the bit lines before forming the contact patterns; and~~

~~planarizing the second conductive film until surfaces of the third insulating film patterns formed on the bit line are exposed.~~

36. (Original) The method of claim 35, wherein the third insulating film pattern has a sufficient thickness to protect the bit lines.

37. – 38. (Canceled)

39. (Currently Amended) A method of manufacturing a semiconductor device comprising:

forming an interlayer dielectric film having pad electrodes therein on a semiconductor substrate;

forming a first insulating film on the interlayer dielectric film; a semiconductor substrate;

forming a patterned conductive layer on the first insulating film;

forming a third insulating film overlying the patterned conductive layer and the first insulating film;

forming contact patterns on the patterned conductive layer, the contact patterns defining contact hole regions therebetween;

forming contact spacers on sidewalls of the contact patterns; and

etching the third insulating film and the first insulating film using the contact patterns and the contact spacers as masks to form the contact holes and to concurrently form third insulating film patterns on sidewalls of the patterned conductive layer.

40. – 41. (Canceled)